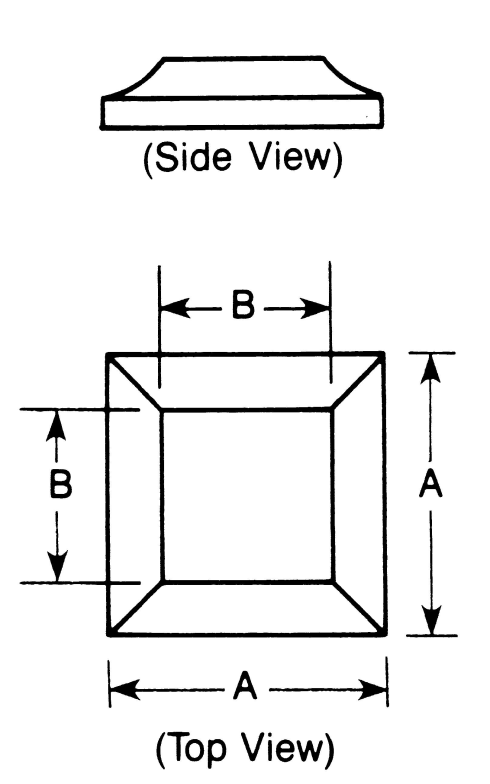
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**.019”**

**.033”**

**.019”**

**CATHODE**

**.033”**

**Top Material: Au**

**Backside Material: Au**

**Bond Pad Size: .019 X .019”**

**Backside Potential: ANODE**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .033” X .033” DATE: 11/3/21**

**MFG: MICROSEMI THICKNESS .007” P/N: 1N4471**

**DG 10.1.2**

#### Rev B, 7/1